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- Neo, Siew  
Santa Clara, California 95051 (UA)
- Chen, Liang-Yuh  
Foster City, California 94404 (US)
- Cheung, Robert  
Cupertino, California 95014 (US)
- Carl, Daniel A.  
Pleasanton, California 94566 (US)
- Shih, Hong  
Walnut, California 91789 (US)

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(71) Applicant: Applied Materials, Inc.  
Santa Clara, California 95054 (US)

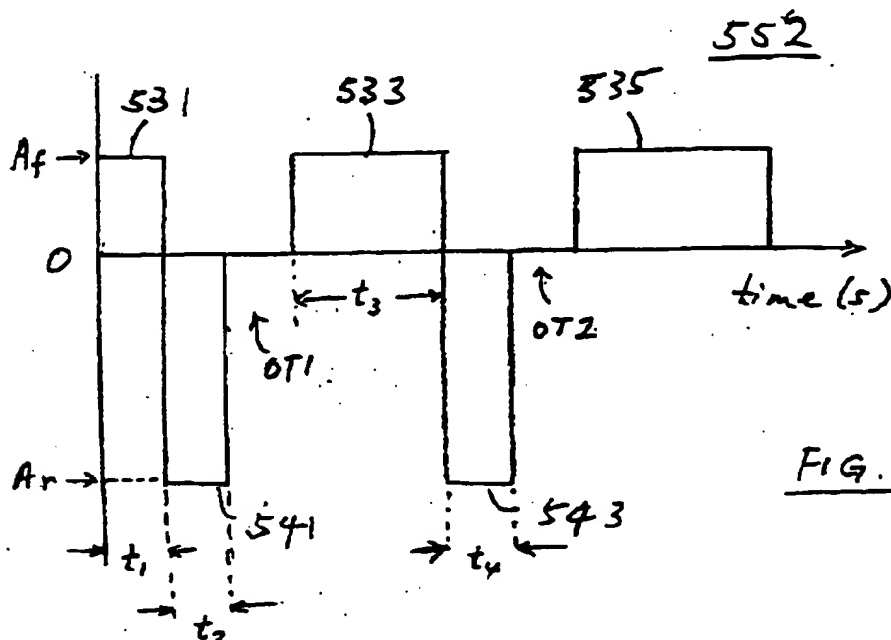
(72) Inventors:  
• Gandikota, Srinivas  
Santa Clara, California 95051 (US)  
• Duboust, Alain  
Sunnyvale, California 94086 (US)

(74) Representative: Käck, Jürgen  
Kahler, Käck, Fiener et Col.  
Vorderer Anger 268  
86899 Landsberg (DE)

(54) Method for electrochemical deposition of metal using modulated waveforms

(57) A method of electrochemical deposition of metal, comprising providing plating waveforms comprising

electrical pulses and at least a time interval of zero voltage or current.



EP 1 132 500 A2

## Descripti n

### CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application, claims priority to commonly-assigned U.S. provisional application, entitled "Method for Electrochemical Deposition of Metal Using Modulated Waveforms," Serial No. 60/187,821, filed March 8, 2000. This application is a continuation-in-part of commonly-assigned copending U.S. application, entitled "Electrochemical Deposition for High Aspect Ratio Structures using Electrical Pulse Modulation," Serial No. 09/569,833, filed May 11, 2000, which claims priority to commonly-assigned U.S. provisional application, entitled "Electrochemical Deposition for High Aspect Ratio Structures using Electrical Pulse Modulation," Serial No. 60/143,361, filed July 12, 1999. All of the above-referenced provisional applications are incorporated herein by reference.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

[0002] The invention relates to electrochemical deposition of a metal.

#### 2. Background of the Related Art

[0003] Sub-quarter micron, multi-level metallization is one of the key technologies for the next generation of ultra large scale integration (ULSI). The multilevel interconnects that lie at the heart of this technology require planarization of interconnect features formed in high aspect ratio apertures, including contacts, vias, lines and other features. Reliable formation of these interconnect features is very important to the success of ULSI and to the continued effort to increase circuit density and quality on individual substrates and die.

[0004] As circuit densities increase, the widths of vias, contacts and other features, as well as the dielectric materials between them, decrease to less than 250 nanometers, whereas the thickness of the dielectric layers remains substantially constant, with the result that the aspect ratios for the features, *i.e.*, their height divided by width, increases. Many conventional deposition processes have difficulty filling structures where the aspect ratio exceeds 4:1, and particularly where the aspect ratio exceeds 10:1. Therefore, there is a great amount of ongoing effort being directed at the formation of void-free, nanometer-sized features having high aspect ratios wherein the ratio of feature height to feature width can be 4:1 or higher. Additionally, as the feature widths decrease, the device current remains constant or increases, which results in an increased current density in the feature.

[0005] Elemental aluminum (Al) and its alloys have been the traditional metals used to form lines and plugs

in semiconductor processing because of aluminum's perceived low electrical resistivity, its superior adhesion to silicon dioxide (SiO<sub>2</sub>), its ease of patterning, and the ability to obtain it in a highly pure form. However, aluminum has a higher electrical resistivity than other more conductive metals such as copper, and aluminum also can suffer from electromigration leading to the formation of voids in the conductor.

[0006] Copper and its alloys have lower resistivities than aluminum and significantly higher electromigration resistance as compared to aluminum. These characteristics are important for supporting the higher current densities experienced at high levels of integration and increased device speed. Copper also has good thermal conductivity and is available in a highly pure state. Therefore, copper is becoming a choice metal for filling sub-quarter micron, high aspect ratio interconnect features on semiconductor substrates.

[0007] Despite the desirability of using copper for semiconductor device fabrication, choices of fabrication methods for depositing copper into very high aspect ratio features, such as 4:1, having 0.35 $\mu$ m (or less) wide vias are limited. As a result of these process limitations, plating, which had previously been limited to the fabrication of lines on circuit boards, is just now being used to fill vias and contacts on semiconductor devices.

[0008] Metal electroplating is generally known and can be achieved by a variety of techniques. A typical method generally comprises depositing a barrier layer over the feature surfaces, depositing a conductive metal seed layer, preferably copper, over the barrier layer, and then electroplating a conductive metal over the seed layer to fill the structure/feature. The deposited layers and the dielectric layers can be planarized, such as by chemical mechanical polishing (CMP), to define a conductive interconnect feature.

[0009] Electroplating or electrochemical deposition is being projected as an economical and viable solution for future copper interconnect needs. FIG. 1 is a simplified sectional view of a fountain plater 10. Generally, the fountain plater 10 includes an electrolyte container 12 having a top opening, a substrate holder 14 disposed above the electrolyte container 12, an anode 16 disposed at a bottom portion of the electrolyte container 12 and a contact ring 20 contacting the substrate 22. A plurality of grooves 24 are formed in the lower surface of the substrate holder 14. A vacuum pump (not shown) is coupled to the substrate holder 14 and communicates with the grooves 24 to create a vacuum condition capable of securing the substrate 22 to the substrate holder 14 during processing. The contact ring 20 comprises a plurality of metallic or semi-metallic contact pins 26 distributed about the peripheral portion of the substrate 22 to define a central substrate plating surface. The plurality of contact pins 26 extend radially inwardly over a narrow perimeter portion of the substrate 22 and contact a conductive seed layer of the substrate 22 at the tips of the contact pins 26. A power supply 30 is electrically

connected to the anode 16 and to the pins 26 thereby providing an electrical bias to the substrate 22. The substrate 22 is positioned above the cylindrical electrolyte container 12 and electrolyte flow impinges perpendicularly on the substrate plating surface during operation of the cell 10.

**[0010]** The electroplating process is typically carried out by applying a constant current density across the substrate plating surface. For example, a constant current density between about 1 and about 60 milliamperes/cm<sup>2</sup> (mA/cm<sup>2</sup>), e.g., about 40 mA/cm<sup>2</sup>, is applied across the substrate plating surface to cause deposition thereon. Since the deposition rate is generally a function of the current density applied over the substrate plating surface, the current density is typically increased, e.g., greater than about 40 mA/cm<sup>2</sup>, to provide faster deposition and increased substrate throughput.

**[0011]** One particular problem encountered in existing electroplating processes is that these electroplating processes have not been able to provide void-free or seam-free fill of high aspect ratio structures. FIG. 2 illustrates a typical deposition result of a high aspect ratio feature 202 on a substrate 200 wherein the mouth/opening 206 of the structure 202 closes off due to overhang or excess deposition of copper at the mouth/opening 206 of the structure 202 - also known as crowning. It has been observed that the deposited metal 210 tends to grow much faster at the mouth or opening 206 of the structure 202, resulting in crowning at the mouth/opening 206 of the structure 202 and leaving a void 204 inside the structure 202, as well as a seam 208. The crowning is accelerated by an increase of the current densities during electroplating, thereby causing even larger voids. It has been observed that voids are also formed in the interconnect features due to grain mismatches from the deposition growth. Furthermore, the presence of the seam 208 may result in void formation during subsequent processing such as substrate annealing.

**[0012]** Therefore, there is a need for a method of electrochemical deposition of a metal into high aspect ratio structures on a substrate that provides void-free and seam-free fill of high aspect ratio structures.

#### SUMMARY OF THE INVENTION

**[0013]** The invention is defined in claims 1, 11, and 16, respectively. Particular embodiments of the invention are set out in the dependent claims.

**[0014]** The present invention provides a method for electrodeposition of a metal on a substrate, comprising applying at least two electrical pulses to the substrate, and providing at least one time interval of zero electrical voltage or current, also known as an "off-time", between the two pulses. In one embodiment, the off-time is provided after a dissolution pulse, while in another embodiment, the off-time is provided after a deposition pulse. In yet another embodiment, off-times are provided after each deposition and dissolution pulses. Void-free and

seam-free deposition of high aspect ratio features can be achieved by optimizing the electrical pulse amplitudes and time durations within a pulse plating waveform.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0015]** The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates a schematic representation of an apparatus suitable for performing electroplating according to the present invention;

FIG. 2 illustrates a schematic cross-sectional view of a typical deposition result of a high aspect ratio feature using prior art techniques;

FIG. 3 illustrates a schematic cross-sectional view of deposition inside a high aspect ratio feature obtained from the present invention;

FIG. 4 illustrates electrical connections for practicing the present invention;

FIGS. 5a-d depict different waveforms for electroplating deposition;

FIG. 6 illustrates a waveform for DC plating incorporating an off-time according to one embodiment of the invention; and

FIG. 7 illustrates a metallization process sequence incorporating the present invention.

**[0016]** To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

#### DETAILED DESCRIPTION OF THE INVENTION

**[0017]** The invention generally provides a method for electrochemical deposition of a metal on a substrate, resulting in void-free and seam-free metal deposition in high aspect ratio structures. In particular, pulse plating is used, in conjunction with the provision of an "off-time" in the plating waveform, to achieve void-free, superfill electroplating of high aspect ratio structures.

**[0018]** The invention can be incorporated within a metallization process sequence such as that shown in FIG. 7. The process sequence 700 of FIG. 7 illustrates several steps in the formation of a metallization structure in a high aspect ratio feature. In step 701, a high aspect ratio feature, e.g., a trench or via, is formed on a substrate such as a semiconductor wafer. The trench or via may be formed by conventional lithographic and etching techniques in an insulating layer that has previously been deposited on the wafer. In step 703, a barrier layer is deposited inside the high aspect ratio feature. The barrier layer, which prevents undesirable diffusion between the underlying substrate and a subsequently deposited metal layer, can be deposited either by chemical

vapor deposition (CVD) or physical vapor deposition (PVD). Optionally, an adhesion layer may also be deposited (not shown in FIG. 7) prior to the formation of the barrier layer.

**[0019]** A seed layer of metal is then deposited, by CVD or PVD, on the barrier layer in step 705. This metal seed layer is typically relatively thin, and is used to facilitate a subsequent electrochemical deposition (or electroplating) performed in step 707. The seed layer metal may be the same as the metal to be deposited in step 707, or another conductive material such as metal nitride, among others. For example, in copper applications, the seed layer may be copper. However, other metals or conductive materials suitable for promoting electroplating can also be used. For example, noble metals or highly conductive metals such as gold, silver, platinum, palladium, nickel, aluminum, tungsten, tin or their alloys are appropriate. When conductive nitrides such as tungsten nitride is used, the nitride layer may also act as a barrier layer.

**[0020]** During step 707, electrochemical plating is performed using a plating solution to deposit a metal layer to a thickness that is at least sufficient to substantially fill the high aspect ratio feature. According to embodiments of the invention, the high aspect ratio feature is filled with the metal in a void-free and seam-free manner by pulse plating techniques using modulated waveforms. In one aspect of the invention, the modulated waveforms comprise electrical pulses of opposite polarities, along with time intervals of zero electrical pulses, or "off-times". The off-times in the plating waveforms allow re-distribution of various chemical species in the plating solution around the high aspect ratio feature to achieve desirable deposition profiles. In another aspect of the invention, pulse plating is used in combination with conventional DC plating to achieve void-free and seam-free metal deposition on the high aspect ratio feature. Although it is generally preferable that the deposition be both void-free and seam-free, it is recognized that void-free deposition alone may suffice for certain applications.

**[0021]** After the formation of the metal layer to a desired thickness, a planarization step 709 may be performed to remove portions of the metal layer that lie outside the high aspect ratio feature, resulting in a planarized metallization structure on the wafer. The planarization may be performed, for example, by chemical mechanical polishing (CMP).

**[0022]** The invention is preferably practiced using an electrochemical deposition cell, such as the Millenia™ Cu ECP system, available from Applied Materials, Inc., Santa Clara, CA. A detailed description of an electrochemical deposition system is provided in commonly assigned and copending U.S. Patent Application 09/289,074, entitled "Electro-chemical Deposition System", filed on April 8, 1999, which is hereby incorporated by reference.

**[0023]** Embodiments of the present invention are

preferably practiced with a copper electroplating bath having multiple components comprising copper electrolyte and additives such as suppressers and accelerators (also called brighteners). A detailed description of the electroplating chemistry, particularly the composition of the electrolyte and additives, is provided in commonly assigned and copending U.S. Patent Application No. 09/245,780, entitled "Electrodeposition Chemistry for Improved Filling of Apertures," filed on February 5, 1999, which is hereby incorporated by reference.

**[0024]** In this exemplary electroplating bath, the copper electrolyte provides the metal ions to be deposited while the suppressers and accelerators control the deposition profile. For example, the suppressers adsorb on the wafer surfaces and inhibit or reduce copper deposition in those areas where suppressers have been adsorbed. Brighteners or accelerators compete with suppresser molecules for adsorption sites and accelerate copper growth in the areas where brighteners or accelerators have been adsorbed.

**[0025]** In one embodiment, the electrolyte comprises copper sulphate, sulphuric acid and chloride ions. The accelerator or catalyst comprises sulphides, which adsorb strongly on copper in the presence of sulphuric acid. The suppressor may be glycol-based, and may comprise, for example, polyethyl glycol (PEG). The suppressor adsorbs on copper and forms an adherent film in the presence of chloride ions. In the areas with adsorbed suppressor, copper deposition is reduced or inhibited. The activities of suppressers and accelerators depend on various parameters such as temperature, pH and chloride concentration in the electroplating bath, and all of these parameters directly or indirectly affect the polarization of these additives.

**[0026]** The suppressers and accelerators tend to reside over the surfaces in the interconnect structures (i.e., vias and trenches) as soon as the substrate comes into contact with the electroplating bath. Since the molecular dimensions of accelerators are much smaller than that of suppressers, the accelerators can diffuse through the electrolyte faster than the suppressers. Crowning may occur when metal deposition is enhanced by accelerators near the opening of the vias or trenches, and metal ions are depleted inside the vias or trenches. According to embodiments of the invention, the off-times in the plating waveforms allow re-distribution of the concentrations of accelerators, suppressers and metal ions, and ensure metal deposition to be achieved without crowning or void formation.

**[0027]** For void-free deposition in a structure with high aspect ratio features (e.g., vias or trenches), it is desirable that electroplating be suppressed at the top of the topographical structure, while accelerated inside the structure. This will promote a bottom-up growth condition, in which the deposition rate at the bottom of the high aspect ratio feature is greater than that towards the opening or sidewall of the feature, resulting in a "super-fill" deposition, which is free of voids or seams. FIG. 3

illustrates schematically a cross-sectional view of a superfilled via structure 302 on a substrate 300. In this illustration, a metal layer 310 is deposited in the via structure 302, or generally a high aspect ratio feature, in a bottom-up growth manner. As such, overhang or excess deposition towards the opening 306 of the via structure 302 is avoided, and a void-free and seam-free metal deposition inside the via structure 302 can be achieved.

[0028] According to embodiments of the invention, various electrical waveforms are used for pulse plating, and desirable plating results such as a superfill profile can be achieved by proper adjustment of the various electrical pulses. The concentration gradients of metal ions, additives or suppressers in the proximity of the high aspect ratio feature are affected by the sequencing and durations of deposition and dissolution pulses. For example, it is believed that the duration of a deposition pulse controls the deposition on the sidewall of the feature, while the dissolution pulse creates additional metal ions and thus, a concentration gradient of these ions, around the feature. By dissolving some deposited metal from the top of the feature, a dissolution pulse (or reverse pulse) allows sufficient time for bottom-up growth within the high aspect ratio feature, without void or seam formation. Furthermore, the deposition and dissolution rates can be controlled by varying the magnitudes of the respective electrical pulses.

[0029] It is recognized by the inventors that a catalytic effect, which affects both the deposition and dissolution reaction, is required to achieve superfill deposition. Thus, it is desirable to facilitate the resorption of accelerators by introducing an off-time after a deposition pulse, or after a dissolution pulse, or between deposition and dissolution pulses. Typically, the time required for resorption of accelerators depend on the bulk solution concentration of the accelerators, and the off-time is adjusted to be on the order of the diffusion time constant of the accelerator molecules. FIG. 4 is a schematic diagram showing the electrical connections for an electroplating system according to embodiments of the invention. A power supply 402 is connected to two electrodes 404 (e.g., anode) and 406 (e.g., cathode) of an electroplating system. The cathode 406 electrically contacts a seed layer 410 on the plating surface 408 of the substrate 430. The power supply 402 preferably includes a control circuit 420 that switches between a constant current operation and a constant voltage operation. The control circuit 420 of the power supply 402 also controls the polarity of the output. The power supply 402 preferably also includes a switching circuit 422 that is programmable to produce a variety of output waveforms, such as an output waveform comprising combinations of a constant voltage or current output for a first duration, a constant voltage or current output for a second duration, and an "off-time" corresponding to zero voltage or current output. The invention contemplates utilizing a variety of power supply designs that are capable of producing such output waveforms and is not limited to any

particular power supply design.

[0030] According to embodiments of the invention, pulse plating is used in conjunction with provisions of an "off-time" to control the deposition and dissolution of metal in the vicinity of the high aspect ratio structure. Although the present discussion focuses on the effect around a high aspect ratio feature, it is recognized that the off-time may also affect metal deposition and dissolution in other areas of the substrate. In pulse plating, electrical pulses - either voltage or current pulses, are applied to the substrate 430 in certain combinations. These pulse combinations may comprise different sequences of pulses of different polarities to achieve metal deposition and dissolution. This contrasts with DC plating, in which a continuous voltage or current is applied to the substrate for a time duration for metal deposition.

[0031] FIG. 5a illustrates a pulse plating waveform 550 having current pulses with different polarities. In this example, current pulses 511 and 513 correspond to deposition pulses, during which copper ions in the electrolyte are accelerated towards the cathode 406, resulting in the plating of copper on the substrate 430. The negative current pulses 521 and 523 correspond to dissolution pulses, during which the copper that has been plated on the substrate 430 is dissolved by being converted into copper ions in the electrolyte. By using different combinations of electrical pulses of opposite polarities, plating of copper can be achieved with varying profiles.

[0032] To achieve superfill in a high aspect ratio structure, e.g., a via or trench, it is desirable to have a higher current density at the bottom than at the top of the structure.

[0033] FIG. 5b illustrates a waveform 552 incorporating the present invention. The waveform 552 comprises electrical pulses of opposite polarities, e.g., 531, 541, 533, 543 and 535. These pulses are characterized by respective time durations  $t_1$ ,  $t_2$ ,  $t_3$  and  $t_4$ . According to the present invention, an "off-time" is provided in the waveform 552 during which, the electrical pulse amplitude is zero. For example, an off-time OT1 is provided between the dissolution pulse 541 and the deposition current pulse 533, while a second off-time OT2 is provided between the dissolution pulse 543 and the deposition pulse 535.

[0034] In general, there are three pulse plating time durations of interest: 1) Deposition time duration; 2) Dissolution time duration; and 3) Off-time. Typically, the specific choices of deposition and dissolution pulse durations depend on the aspect ratios of the structures to be filled, and process optimization may involve, for example, varying the ratio of the deposition pulse duration to the dissolution pulse duration. After a deposition pulse, a concentration gradient of copper ions is created inside the via due to the consumption of copper ions. It is found that if the copper ion distribution and the concentration gradient of additives generated during the dissolution step are not balanced, crowning or void for-

mation can occur.

[0035] Therefore, the durations of the off-time OT1 and OT2 are selected to establish proper concentration gradients, or redistribution of the various copper or additive species in the vicinity of the structure. For example, the off-time duration may be selected to be on the order of the diffusion time constant of a certain species of interest. The diffusion time  $\tau$  for any of the species in the electroplating bath may be approximated by:  $\tau = h^2/D$ , where  $h$  represents the depth of the via and  $D$  represents the diffusivity of the species. In one embodiment, electroplating is performed on vias having a depth of about 1.6  $\mu\text{m}$ . With the electroplating bath used in this embodiment, the diffusivity of the additives is believed to be one or two orders of magnitudes lower than that of copper. For a 1.6  $\mu\text{m}$  via, for example, the diffusion time for additives is estimated to be about 50 milliseconds (ms). Thus, an off-time duration of about 100 ms may be selected in the plating waveform, to allow for a sufficiently long time for the additives to diffuse and establish the proper concentration distribution for a void-free and seam-free filling of the via. Note that since diffusion is a function of temperature, the specific bath temperature may also affect the choice of the off-time durations OT1 and OT2. In general, since the molecular dimensions of catalysts or accelerators are smaller than that of the suppressers, the diffusion of catalysts is also faster than that of suppressers.

[0036] In the illustrative embodiment of FIG. 5b, the forward current or voltage (*i.e.*, for deposition) for the pulses 531, 533 and 535 has a lower amplitude ( $A_f$ ) than the amplitude ( $A_r$ ) of the reverse current or voltage used for the dissolution pulses 541 and 543. This arrangement tends to reduce the formation of voids. Although each electrical pulse shown in FIG. 5b has a constant amplitude within the pulse duration, it is also possible to use plating pulses with amplitudes that are ramped as a function of time. In addition, it is not necessary that all deposition (or dissolution) pulses have the same amplitudes within one plating waveform.

[0037] FIGS. 5c-5d illustrate other variations of waveforms incorporating the present invention. FIG. 5c, for example, shows a waveform 554 having off-time intervals OT3 and OT4 after respective positive pulses 571 and 573 but before respective negative pulses 561 and 563. FIG. 5d illustrates a waveform 556 that provides off-time intervals OT5, OT6, OT7 and OT8 before and after each electrical pulse 591, 581, 593, 583 and 595, regardless of polarities. It should be noted that, in general, the time durations of each pulse and the off-time may be different from each other, and can be adjusted according to specific desired profiles or properties of the deposited metal. For example, the off-time duration may range from about 1 ms to about 500 ms. The pulse duration for a deposition (cathodic) pulse may range from about 500 ms to about 3000 ms, while that for a dissolution pulse (anodic) may range from about 1 ms to about 300 ms. The choice of the pulse durations de-

pends on the width and aspect ratio of the feature, as well as on the current densities used. For example, a smaller feature (or higher aspect ratio) would typically require a lower ratio of deposition pulse duration to dissolution pulse duration. The amplitude of a deposition pulse is typically in the range of about 0.5 Amp to about 10 Amp, while that of a dissolution pulse may range from about 3 Amp to about 60 Amp. The magnitudes of deposition and dissolution current densities are determined based on various considerations such as the requirement for superfill profile and process throughput, among others.

[0038] In addition, the use of an off-time may also be combined with DC plating, as illustrated in FIG. 6, which shows deposition pulses 601, 603 of one polarity followed by respective off-time durations 602, 604. A DC current density of between about 1 and about 60 milliamperes/cm<sup>2</sup> may be used. Alternatively, the desired via fill may be performed by pulse plating using multiple cycles of deposition and dissolution pulses, with or without off-times, followed by electroplating to the required total copper thickness using DC plating."

#### Example

[0039] An example is given below of copper electroplating according to one embodiment of the invention on a substrate having high aspect ratio interconnect features. Prior to electroplating, a barrier layer comprising about 250Å of tantalum nitride is deposited by physical vapor deposition over the substrate using processing parameters that are known in the art. Preferably, the barrier layer is deposited using a Vectra IMP™ chamber from Applied Materials, Inc., Santa Clara, California. A copper seed layer having a thickness of about 2000Å is formed on the barrier layer, using, for example, known processing parameters for physical vapor deposition. The substrate is then transferred to an electroplating cell, *e.g.*, a Millenia™ ECP system, available from Applied Materials, Inc., for copper electroplating.

[0040] In this embodiment, the electroplating bath comprises 0.85M copper sulphate, appropriate additives (suppressers and accelerators) and chloride ions at about 60 to about 70 ppm, with a bath pH of about 1.0 at a temperature of about 15°C. The additives, accelerator "X" and suppresser "Y" were supplied by Lea Ronal (or Shipley Ronal) of New York, and are known as Electra plate X Rev 1.0 and Electra plate Y Rev 1.0, which is also known as SB additive. The plating waveform comprises a deposition pulse having an amplitude of about 3 Amp and a duration of about 3 s, a negative pulse (dissolution) duration of about 100 ms and an amplitude of between about 25 Amp to about 40 Amp, preferably about 30 Amp, along with an off-time duration of about 100 ms after the dissolution pulse. For example, about 15 to about 20 cycles (comprising a sequence of deposition, dissolution and off-time) are used to achieve void-free filling of 1.6  $\mu\text{m}$  deep, sub-0.25  $\mu\text{m}$  vias. It is

also observed that hydrogen given off during the dissolution pulse may be trapped inside the vias of the wafer. Thus, it is generally desirable to incorporate an off-time after the dissolution pulse that is sufficiently long to allow for hydrogen to escape from the vias.

[0041] Although several preferred embodiments which incorporate the teachings of the present invention have been shown and described in detail, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

## Claims

1. A method for electroplating a metal on a substrate, comprising the steps of:

(a) applying a first electrical pulse to the substrate;  
 (b) providing a time interval of zero electrical pulse after the first electrical pulse; and  
 (c) applying a second electrical pulse to the substrate.

2. The method of claim 1, wherein the first electrical pulse has a negative polarity.

3. The method of claim 1, wherein the first electrical pulse and the second electrical pulse have opposite polarities.

4. The method of claim 1, wherein the time interval of zero electrical pulse is between about 1 and 500 milliseconds.

5. The method of claim 2, wherein the first electrical pulse is a current pulse having an amplitude between about 3 and about 60 amperes.

6. The method of claim 2, wherein the first electrical pulse has a time duration between about 1 and about 300 milliseconds.

7. The method of claim 3, wherein the first electrical pulse is a deposition pulse during which metal is deposited on the substrate.

8. The method of claim 7, wherein the deposition pulse has an amplitude between about 0.5 and about 10 amperes.

9. The method of claim 7, wherein the deposition pulse has a time duration between about 500 and about 3000 milliseconds.

10. The method of claim 1, further comprising the steps of:

(d) providing a time interval of zero electrical pulse after the second electrical pulse to the substrate;

(e) applying a third electrical pulse to the substrate;

wherein the first electrical pulse and the third electrical pulse are deposition pulses and the second electrical pulse is a dissolution pulse.

11. A method for depositing a metal on a substrate, comprising the steps of:

(a) providing a sequence of electrical pulses to the substrate; and  
 (b) providing a time interval of zero electrical pulse between each of the electrical pulses in the sequence.

12. The method of claim 11, wherein the sequence of electrical pulses are deposition pulses.

13. The method of claim 11, wherein successive pulses in the sequence of electrical pulses have opposite polarities.

14. The method of claim 11, wherein the steps (a) and (b) are performed with the substrate in an electroplating bath comprising a chemical having a diffusion time constant about equal to the time interval of zero electrical pulse.

15. The method of claim 14, wherein the electroplating bath further comprises copper ions.

16. A method for electroplating a metal on a substrate having a trench, comprising the steps of:

(a) applying a first electrical pulse having a first polarity to the substrate;  
 (b) applying a second electrical pulse to the substrate, wherein the second electrical pulse has a second polarity opposite to the first polarity of the first electrical pulse;  
 (c) repeating steps (a) and (b) for a plurality of cycles to deposit the metal inside the trench; and  
 (d) applying a DC current to the substrate to deposit the metal to a desired thickness on the substrate.

17. The method of claim 16, further comprising the step of providing a time interval of zero electrical pulse between the first and the second electrical pulses.

18. The method of claim 16, wherein the first electrical pulse has a negative polarity, a pulse duration of about 100 milliseconds and a pulse amplitude of

about 25 Amperes.

19. The method of claim 17, wherein the time interval of zero electrical pulse is about 100 milliseconds.

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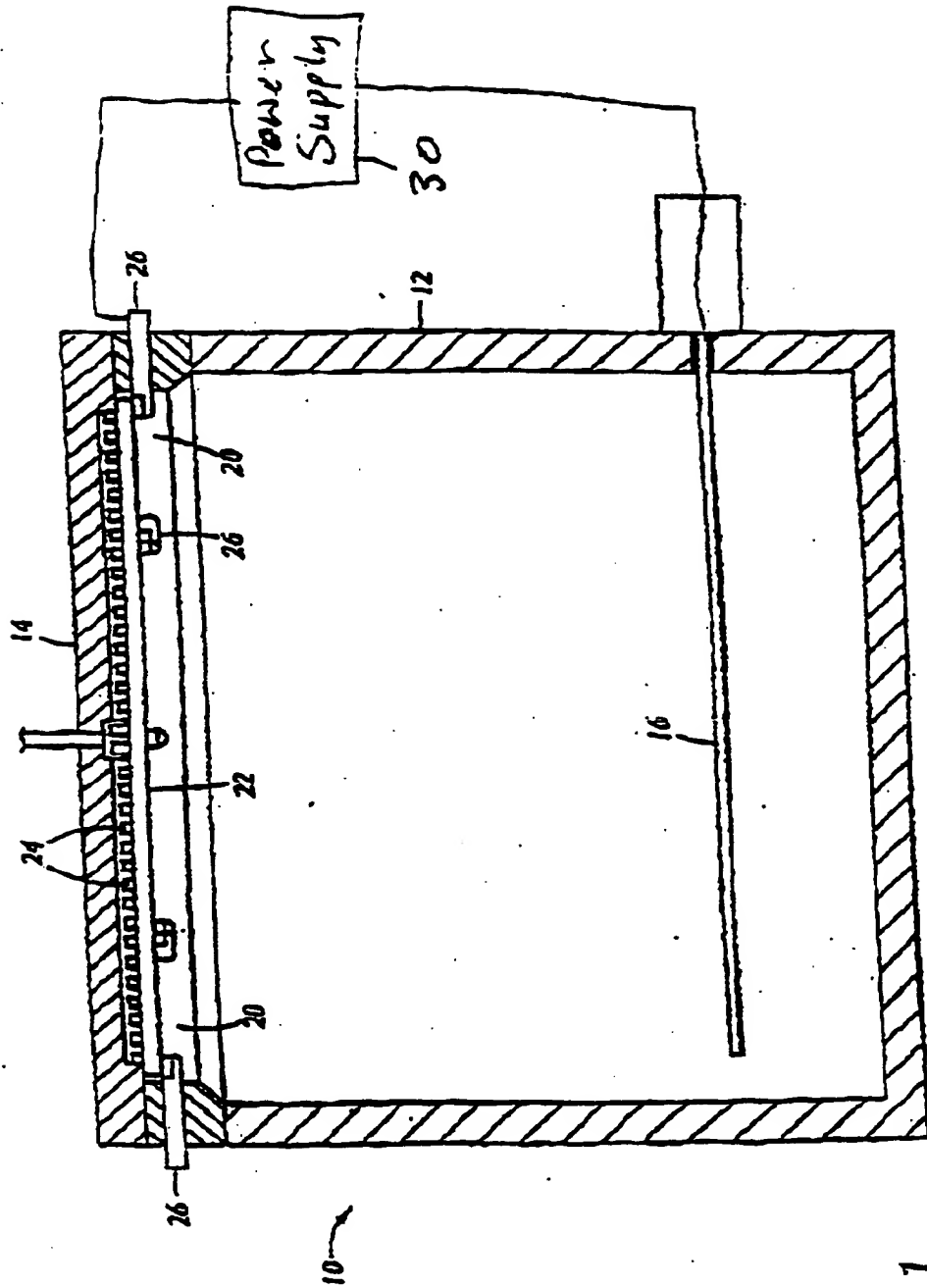


Fig. 1  
(PRIOR ART)

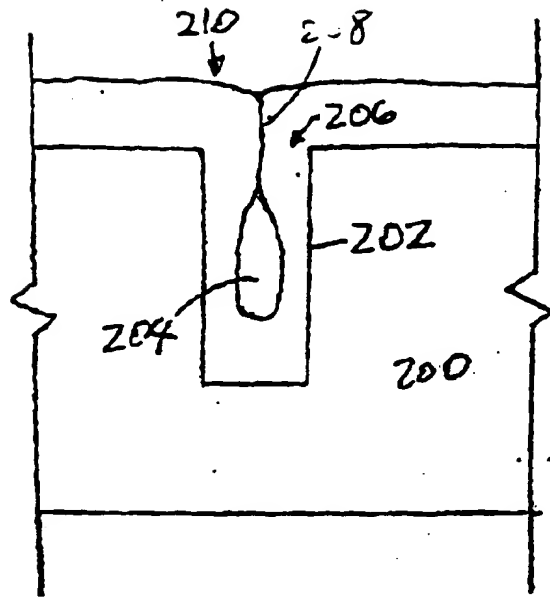


Figure 2 (prior art)

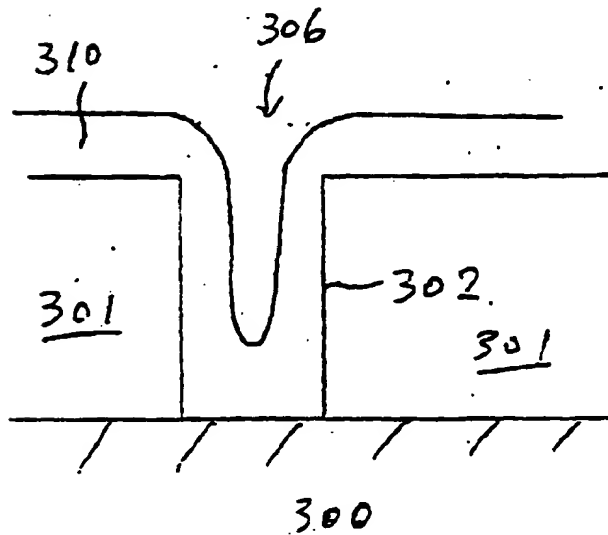


FIG. 3

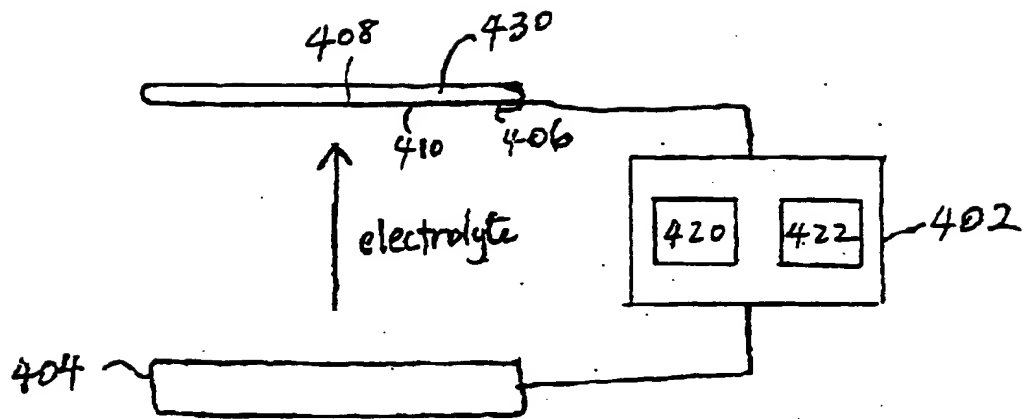
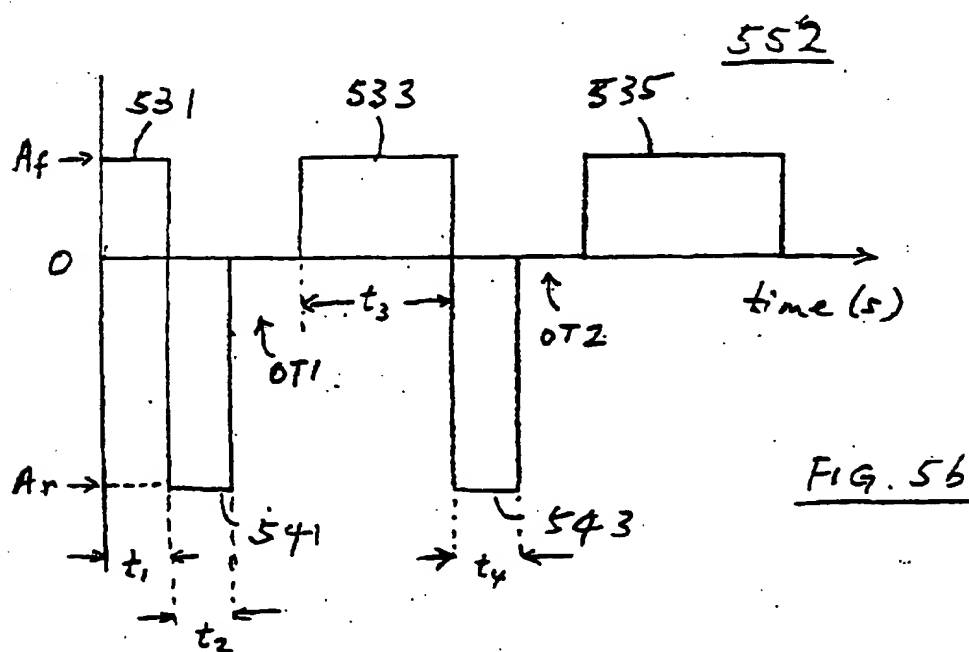
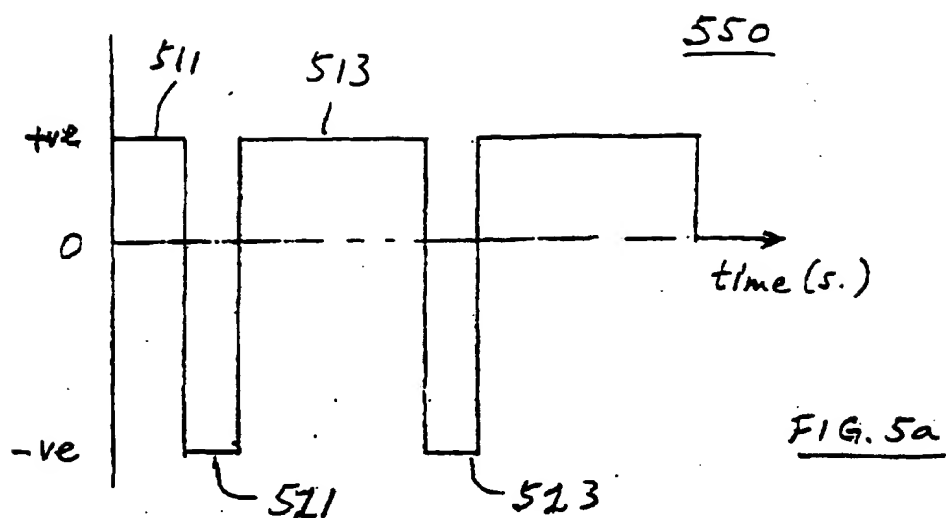
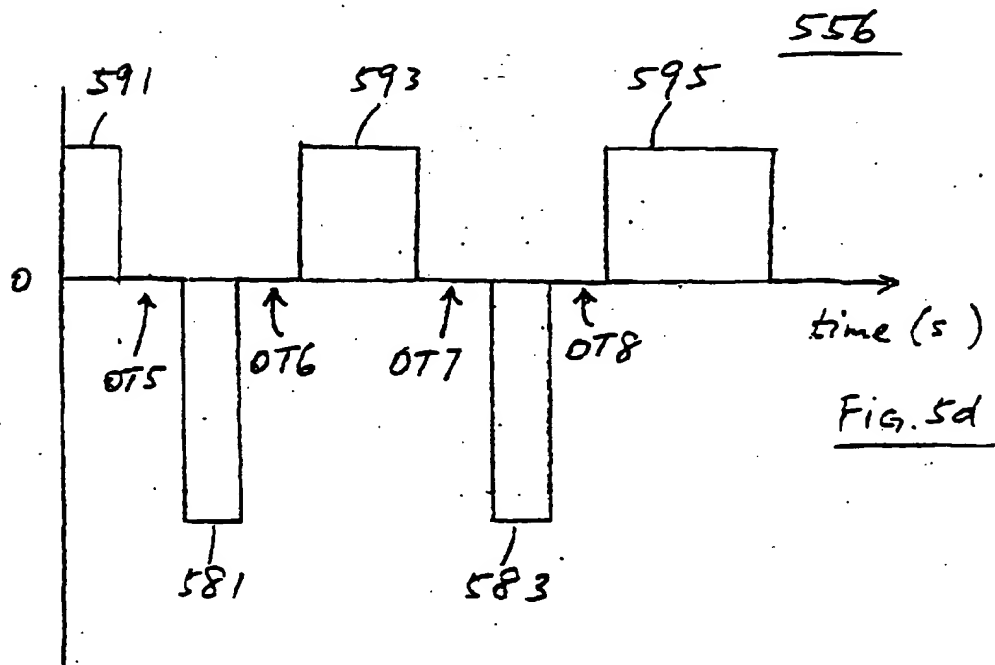
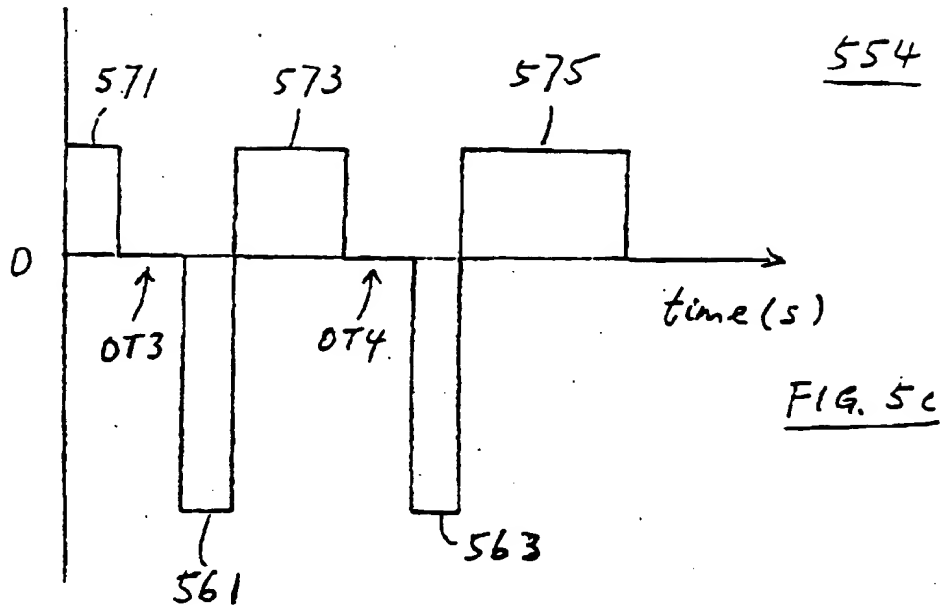


FIG. 4





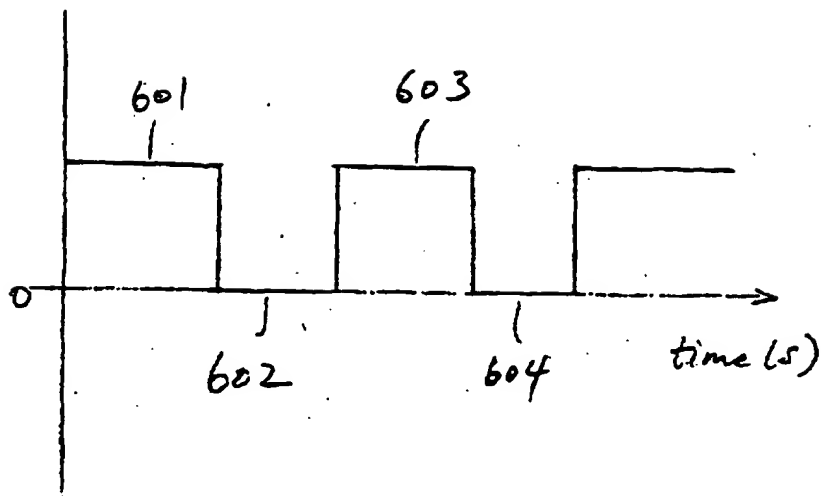


FIG. 6

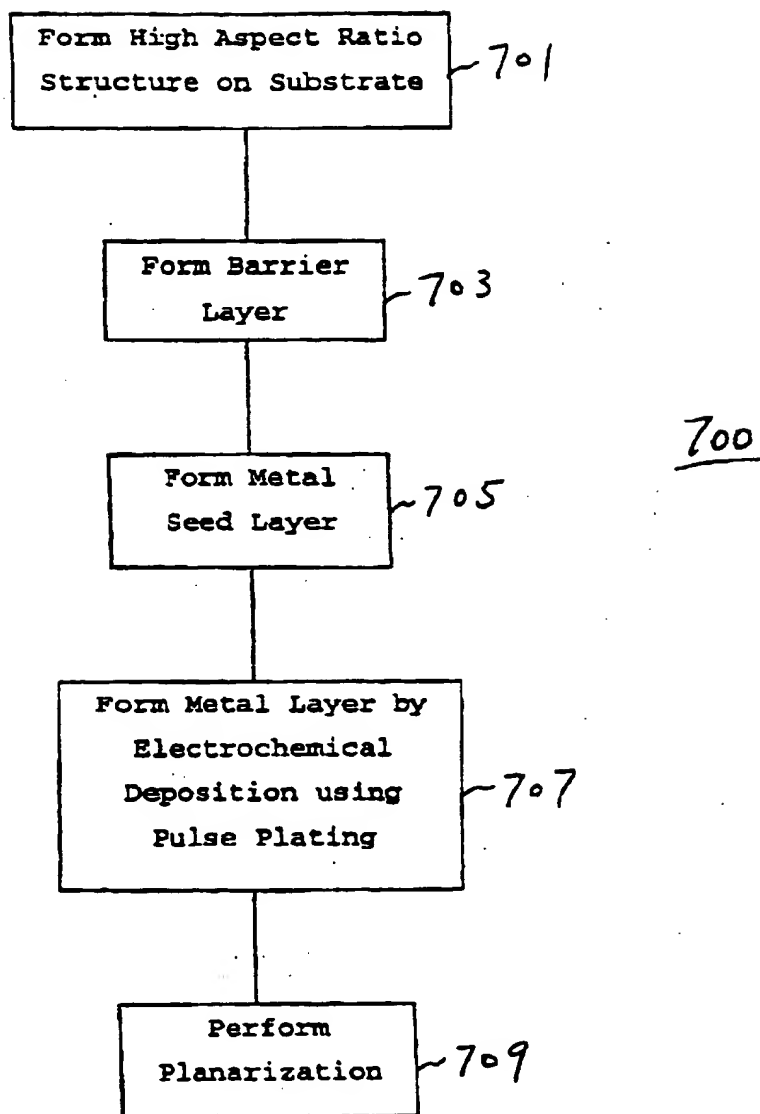


FIG. 7







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(71) Applicant: **Applied Materials, Inc.**  
**Santa Clara, California 95054 (US)**

(72) Inventors:  
• **Gandikota, Srinivas**  
**Santa Clara, California 95051 (US)**

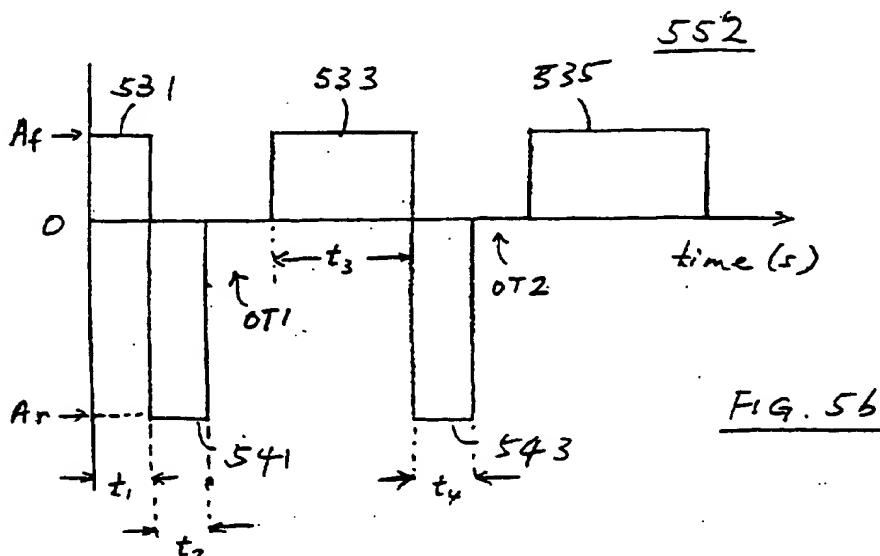
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Sunnyvale, California 94086 (US)
- Neo, Siew  
Santa Clara, California 95051 (UA)
- Chen, Liang-Yuh  
Foster City, California 94404 (US)
- Cheung, Robert  
Cupertino, California 95014 (US)
- Carl, Daniel A., c/o Law Department, MS 2061  
Santa Clara, California 95052 (US)
- Shih, Hong  
Walnut, California 91789 (US)

(74) Representative: **Käck, Jürgen**  
**Kahler, Käck, Fiener et Col. Vorderer Anger 268**  
**86899 Landsberg (DE)**

**(54) Method for electrochemical deposition of metal using modulated waveforms**

(57) A method of electrochemical deposition of metal, comprising providing plating waveforms comprising

electrical pulses and at least a time interval of zero voltage or current.



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Office

# EUROPEAN SEARCH REPORT

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The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>30 November 2001</b>	Examiner <b>Van Leeuwen, R</b>
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